	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	238	(sacrificial) same (hard adj mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 10:06
2	BRS	L2	198	1 same (etch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 10:07
3	BRS	L3	134	2 same silicon	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 10:46
4	BRS	L4	1617	((plasma or dry) adj3 etch$3) with (sacrificial or resist$3 or photoresist$3) with ((hard adj3 mask) or SiN or SiON or (silicon adj nitride) or (silicon adj oxynitride))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 10:50
5	BRS	L5	131	4 with polysilicon	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 13:25

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	IS&R	L7	300	(438/695).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 14:14
7	IS&R	L6	184	(438/9).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 13:28
8	BRS	L13	574	single adj3 etch$3 adj3 process	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 14:18
9	BRS	L14	0	13 with sacrificial with (hard adj mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 14:19
10	BRS	L15	7	13 with sacrificial	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 14:20

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	IS&R	L16	301	(438/697).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/26 14:53

L1 nitride or oxynitride or hard near3 mask$4

L2 Photoresist or resist or BARC

L3 (L1 near8 L2) near8 (remov$4 or etch$4 or strip$4) 1 near4 [(plasma complete$4 or all or total$3 or entire - - -) or (single or one) near2 step]

438/738

717

DOCUMENT-IDENTIFIER: US 20020117706 A1

TITLE: Non-volatile semiconductor memory device and method of manufacturing the same

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[0081] After application of a photoresist 19 on silicon nitride film 18 by photolithography, photoresist 19 is patterned into a predetermined shape. Using this **photoresist** 19 as a mask, as shown in FIG. 3, **silicon nitride** film 18, doped **polysilicon** film 6 and thermal oxide film 4 are **dry-etched**.

[0082] After removal of **photoresist** 19, using **silicon nitride** film 18, doped **polysilicon** film 6 and thermal oxide film 4 as a mask (mask film), semiconductor substrate 1 is **dry-etched**.

[0125] Next, doped polysilicon film 6 and silicon nitride film 18 are deposited by a technique similar to the first embodiment, and a photoresist 28 in a predetermined shape is formed on silicon nitride film 18 by photolithography. As shown in FIG. 18, using this **photoresist** 28 as a mask, **silicon nitride** film 18, doped **polysilicon** film 6, thermal oxide film 4 and thermal oxide film 5 are **dry-etched**. Thus, a region where the trench for element-isolation is to be formed is exposed in the memory cell portion and the peripheral circuit portion.

[0126] After removal of **photoresist** 28, using the patterned **silicon nitride** film 18, doped **polysilicon** film 6, thermal oxide film 4 and thermal oxide film

5 as a mask, semiconductor substrate 1 is **dry-etched**. This forms trenches 3
and 29 each having a depth of about 400 nm as shown in FIG. 19.